Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A high data rate wireless receiver for an FSK data transceiver system having a data transfer protocol, and a carrier signal having a pair of carrier frequencies, the receiver having a signal path and including a digital FSK demodulator for demodulating an FSK signal by measuring the period of incoming carrier signal cycles using a high frequency local clock time-base, f_{TB}, the FSK demodulator demodulating the FSK signal having a data rate from the carrier signal, the digital FSK demodulator generating a serial data bit stream based on the FSK carrier signal and generating a synchronized constant frequency clock signal from the carrier frequencies based on the data transfer protocol for sampling the serial data bit stream wherein the frequency of the local clock time-base is substantially higher than the carrier frequencies to digitally measure periods of each received half cycle of the FSK carrier signal wherein the demodulator discriminates between carrier frequencies regardless of data rate and wherein the data transfer protocol, the FSK demodulator and the receiver are all fully digital without the need for analogue circuits in the signal path of the receiver to make the system small, low power and robust.

2. (Previously Presented) The receiver as claimed in claim 1, wherein the data rate is greater than one million bits per second.

3. (Previously Presented) The receiver as claimed in claim 1, wherein the data rate approximates the carrier frequencies.

4. (Currently Amended) The receiver as claimed in claim 1, wherein the carrier frequency is ~~less than about 25 megahertz and~~ more than about 1 megahertz.

5. (Previously Presented) The receiver as claimed in claim 1, wherein one of the carrier frequencies is twice the other carrier frequency so that a duration of each data bit is substantially the same, independent of its value.

6. (Previously Presented) The receiver as claimed in claim 1, wherein the receiver also detects an error in the FSK carrier signal based on the protocol and provides a corresponding error signal.

7. (Currently Amended) The receiver as claimed in claim 1, wherein the receiver [[also]] digitally measures the period of each received half cycle of the FSK carrier signal to obtain a series of pulses which distinguish between long and short FSK carrier cycles.

8. (Previously Presented) The receiver as claimed in claim 7, wherein the receiver includes an n-bit counter that runs with a clock time-base, f_{TB}, having a substantially constant frequency at a rate substantially higher than the FSK carrier frequencies, f_1 and f_0, to digitally measure the periods.

9. (Previously Presented) The receiver as claimed in claim 1, wherein the system is a magnetically powered wireless system.

10. (Currently Amended) The receiver as claimed in <u>claim</u> 9, wherein the receiver is a wireless biomedical implant.

11. (Currently Amended) A chip for an FSK data transceiver system having a fully digital data transfer protocol and a carrier signal having a pair of carrier frequencies, the chip comprising:

a substrate; and

a receiver having a signal path and including a digital FSK demodulator formed on the substrate for demodulating an FSK signal by measuring the period of incoming carrier signal cycles <u>using a high frequency local time-base f_{TB}</u>, the FSK demodulator demodulating the FSK signal having a data rate from the carrier signal wherein the receiver generates a serial data bit stream based on the received FSK carrier signal and generates a synchronized constant frequency clock signal from the carrier frequencies based on the data transfer protocol for sampling the serial data bit stream <u>wherein the frequency of the local clock time-base is substantially higher than the carrier frequencies to digitally measure periods of each received half</u>

cycle of the FSK carrier signal wherein the demodulator discriminates between carrier frequencies regardless of data rate and wherein the receiver is fully digital without the need for analogue circuits in the signal path of the receiver to minimize the power consumption and the amount of surface area occupied by the demodulator on the substrate and to make the system robust.

12. (Original) The chip as claimed in claim 11, wherein the data rate is greater than one million bits per second.

13. (Original) The chip as claimed in claim 11, wherein the data rate approximates the carrier frequencies.

14. (Currently Amended) The chip as claimed in claim 11, wherein the carrier frequency is ~~less than about 25 megahertz and~~ more than about 1 megahertz.

15. (Previously Presented) The chip as claimed in claim 11, wherein one of the carrier frequencies is twice the other carrier frequency so that a duration of each data bit is substantially the same, independent of its value.

16. (Previously Presented) The chip as claimed in claim 11, wherein the receiver also detects an error in the FSK carrier signal based on the protocol and provides a corresponding error signal.

17. (Previously Presented) The chip as claimed in claim 11, wherein the demodulator also digitally measures the period of each received half cycle of the FSK carrier signal to obtain a series of pulses which distinguish between long and short FSK carrier cycles.

18. (Previously Presented) The chip as claimed in claim 17, wherein the demodulator includes an n-bit counter that runs with a clock time-base f_{TB}, having a substantially constant frequency at a rate substantially higher than the FSK carrier frequencies, f_1 and f_0, to digitally measure their periods.

19. (Original) The chip as claimed in claim 11, wherein the system is a magnetically powered wireless system.

20. (Currently Amended) A method for receiving and demodulating an FSK signal having a data rate from a carrier signal having a pair of carrier frequencies in an FSK transceiver system having a receiver signal path, the system having a digital data transfer protocol, the method comprising:

digitally measuring the period of each received positive half cycle of the FSK carrier signal using a high frequency local clock time-base, f_{TB} to obtain a series of pulses which distinguish between long and short FSK carrier cycles;

digitally generating a serial data bit stream based on the FSK carrier signal and the series of pulses; and

digitally generating a synchronized constant frequency clock signal from the carrier frequencies based on the digital data transfer protocol and the series of pulses wherein the frequency of the local clock time-base is substantially higher than the carrier frequencies to digitally measure periods of each received half cycle of the FSK carrier signal wherein the demodulator discriminates between carrier frequencies regardless of data rate and wherein the method is performed in a fully digital fashion without the need to perform any steps in the signal path in an analogue fashion to make the system small, low power and robust.